IN THE SPECIFICATION

The paragraph beginning at page 4, line 27 amended as follows:

Fine delay segment 120 connects to coarse delay segment 110 at node 111 to receive the Cout signal. Fine delay segment 120 includes a plurality of fine delay elements (D) 122, 124 and 126 connected in a cascading fashion to form a plurality fine delay paths 131, 132, 133 and 134. In the embodiment represented by Figure 1, each of the fine delay elements 122, 124 and 126 is represented by delay element 200 shown in Figure 2 which includes two inverters 202 and 204 connected in series. Fine delay segment 120 further includes a selector or multiplexor (MUX) 130, and a shift register 150.

The paragraph beginning at page 6, line 17 amended as follows:

A shift register 150 connects to select lines 141, 142, 143 and 144 to provide the select signals SA, SB, SC and SD to MUX 130. Shift register 150 includes a plurality of register cells (C) 151, 152, 153 and 154. Each of the register cells 151-154 holds a logic value such as logic 0 or logic 1. Each of the register cells 151-154 includes an output connected to one of the select lines 141, 142, 143 and 144 to provide one of the SA, SB, SC and SD signals. Shift register 150 receives shifting signals, generated by phase detector 180, on lines 160 and 162. The shifting signals includes a shift left signal (SL) provided on line 160 and a shift right signal (SR) provided on line 162.

The paragraph beginning at page 18, line 1 is amended as follows:

A novel delay locked loop (DLL) has been disclosed [[DLL]]. The DLL generates an internal clock signal by delaying an external clock signal with a coarse delay and a fine delay. The coarse delay includes a number of coarse unit delays within a coarse delay range; the fine delay includes a number of fine unit delays within a fine delay range. A fine unit delay is smaller than a coarse unit delay. To keep the external and internal clock signals synchronized, the DLL adjusts the fine delay then the coarse delay by increasing or decreasing the numbers of fine unit delays and coarse unit delays. The coarse delay is adjusted only when the fine delay is at a minimum or maximum delay of the fine delay range and an increase or decrease in delay is needed respectively. Since the fine unit delay is smaller than the coarse unit delay, adjusting the

fine delay before adjusting the coarse delay reduces the chance of overshoot or undershoot a target delay. Therefore, the accuracy of the timing relationship between external and internal clock signals is improved.